

LH52A512

PRELIMINARY
CMOS 512K (64K × 8) Static Ram

FEATURES

- 64K × 8 bit organization
- Access time: 70/100 ns (MAX.)
- Current consumption:
 - Operating: 385 mW (MAX.)
 - 110 mW (t_{RC} , $t_{WC} = 1 \mu s$)
 - Standby: 275 μW (MAX.)
 - Data retention:
 - 3 μW ($V_{CC} = 3 V$, $T_A = 25^\circ C$)
 - 9 μW ($V_{CC} = 3 V$, $T_A = 40^\circ C$)
- Single 5 V power supply: 5 V $\pm 10\%$
- Fully-static operation
- TTL compatible I/O
- Three-state outputs
- Operating temperature: 0°C to +70°C
- Packages:
 - 32-pin, 525-mil SOP
 - 32-pin, 8 × 20 mm² TSOP (Type I)

DESCRIPTION

The LH52A512 is a static RAM organized as 64K × 8 bits. An efficient design is obtained with a CMOS periphery and a matrix constructed with polysilicon load memory cells.

PIN CONNECTIONS

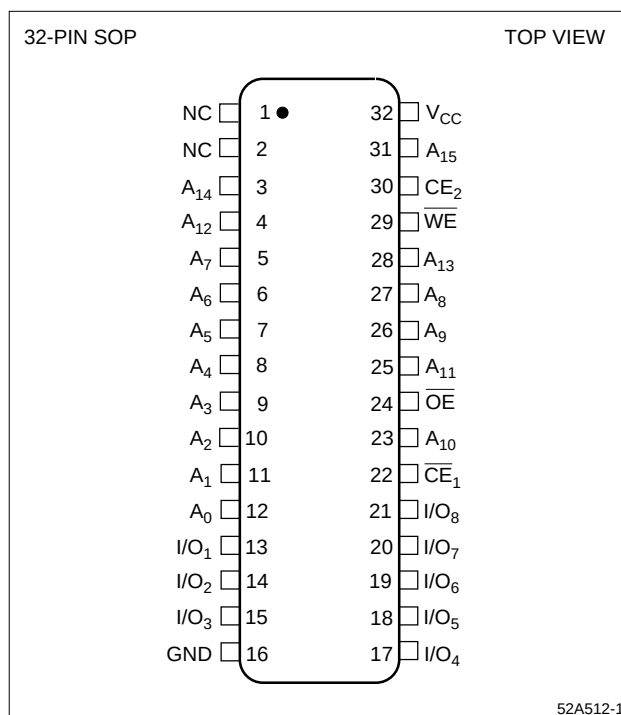


Figure 1. Pin Connections for SOP Package

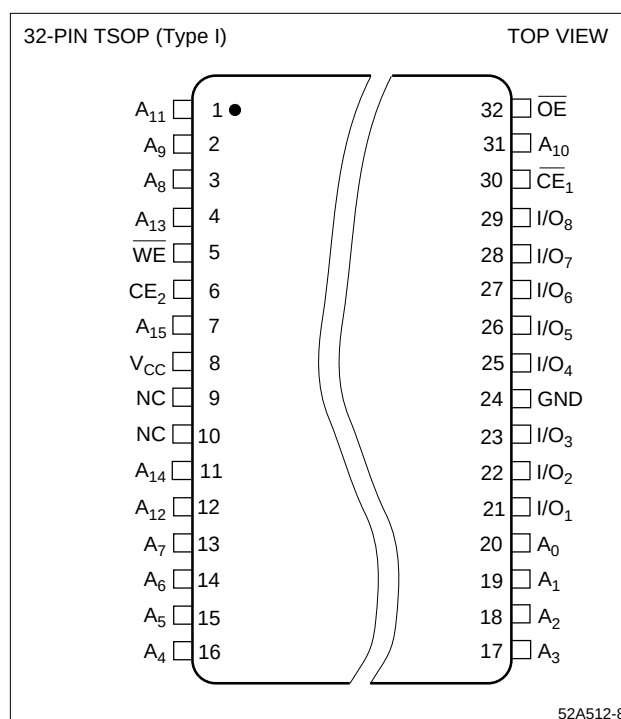
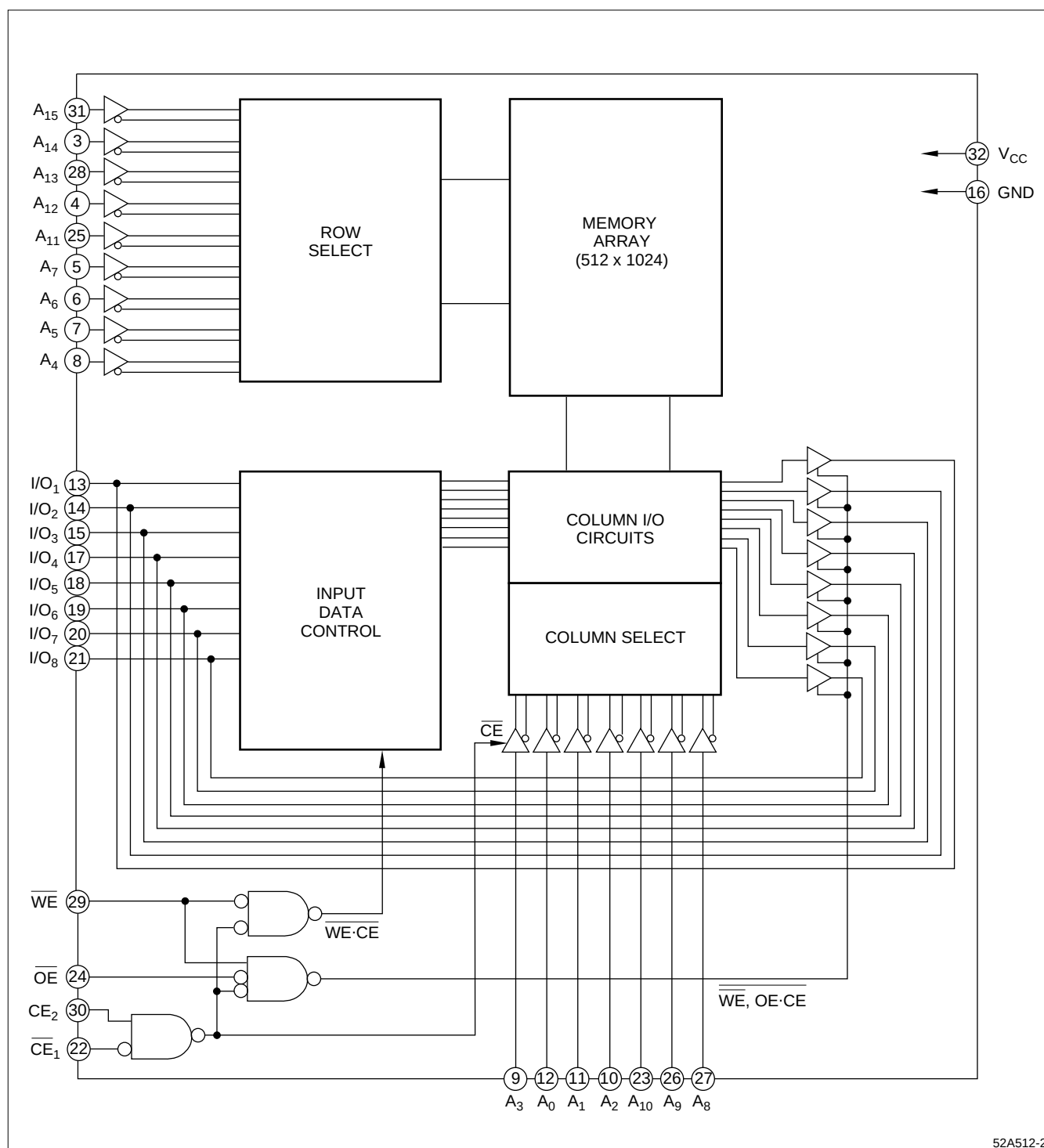


Figure 2. Pin Connections for TSOP Package



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Figure 3. LH52A512 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A ₀ - A ₁₅	Address inputs
$\overline{CE}_1$	Chip Enable input 1
CE ₂	Chip Enable input 2
$\overline{WE}$	Write Enable input
OE	Output Enable input

SIGNAL	PIN NAME
I/O ₁ - I/O ₈	Data inputs and outputs
V _{CC}	Power supply
GND	Ground
NC	No connection

TRUTH TABLE

$\overline{CE}_1$	CE_2	$\overline{WE}$	$\overline{OE}$	MODE	I/O ₁ - I/O ₈	SUPPLY CURRENT	NOTE
H	X	X	X	Deselect	High-Z	Standby (I _{SB})	1
X	L	X	X	Deselect	High-Z	Standby (I _{SB})	1
L	H	L	X	Write	D _{IN}	Operating (I _{CC})	1
L	H	H	L	Read	D _{OUT}	Operating (I _{CC})	
L	H	H	H	Output disable	High-Z	Operating (I _{CC})	

NOTE:

1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V _{CC}	−0.5 to +7.0	V	1
Input voltage	V _{IN}	−0.5 to V _{CC} + 0.3	V	1, 2
Operating temperature	T _{opr}	0 to +70	°C	
Storage temperature	T _{stg}	−65 to +150	°C	

NOTES:

1. The maximum applicable voltage on any pin with respect to GND.
2. Undershoot of −3.0 V is allowed for pulse width below 50 ns.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Supply voltage	V _{CC}	4.5	5.0	5.5	V	
Logic '1' input voltage	V _{IH}	2.2		V _{CC} + 0.3	V	
Logic '0' input voltage	V _{IL}	−0.3		0.8	V	1

NOTE:

1. Undershoot of −3.0 V is allowed for pulse width below 50 ns.

DC CHARACTERISTICS¹ ($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT
Input leakage current	I_{LI}	$V_{IN} = 0\text{ V to }V_{CC}$	-1.0	1.0	μA
Output leakage current	I_{LO}	$\overline{CE}_1 = V_{IH}$ or $CE_2 = V_{IL}$ or $OE = V_{IH}$ or $WE = V_{IL}$ $V_{I/O} = 0\text{ V to }V_{CC}$	-1.0	1.0	μA
Operating supply current	I_{CC1}	Minimum cycle, $V_{IN} = V_{IL}$ or V_{IH} $CE_1 = V_{IL}$, $CE_2 = V_{IH}$, $I_{I/O} = 0\text{ mA}$		70	mA
Standby current	I_{SB}	$CE_2 \leq 0.2\text{ V}$ or $\overline{CE}_1, CE_2 \geq V_{CC} - 0.2\text{ V}$		50	μA
	I_{SB1}	$\overline{CE}_1, CE_2 = V_{IH}$ or $CE_2 = V_{IL}$		3	mA
Output voltage	V_{OL}	$I_{OL} = 2.1\text{ mA}$		0.4	V
	V_{OH}	$I_{OH} = -1.0\text{ mA}$	2.4		

READ CYCLE ($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$)

PARAMETER	SYMBOL	-70 ns		-100 ns		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	70		100		ns	
Address access time	t_{AA}		70		100	ns	
$\overline{CE}_1$ Low to valid data	t_{ACE1}		70		100	ns	
CE_2 High to valid data	t_{ACE2}		70		100	ns	
$\overline{OE}$ Low to valid data	t_{OE}		40		50	ns	
Output hold from address change	t_{OH}	10		10		ns	
$\overline{CE}_1$ Low to output active	t_{CLZ1}	10		10		ns	1
CE_2 High to output active	t_{CLZ2}	10		10		ns	1
$\overline{OE}$ Low to output active	t_{OLZ}	5		5		ns	1
$\overline{CE}_1$ High to output in High-Z	t_{CHZ1}		30		35	ns	1
CE_2 Low to output in High-Z	t_{CHZ2}		30		35	ns	1
$\overline{OE}$ High to output in High-Z	t_{OHZ}		30		35	ns	1

NOTE:

- Active output to high-impedance and high-impedance to output active tests specified for a $\pm 200\text{ mV}$ transition from steady state levels into the test load.

WRITE CYCLE ($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$)

PARAMETER	SYMBOL	–70 ns		–100 ns		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
Write cycle time	t_{WC}	70		100		ns	
$\overline{CE}_1$ Low to end of write	t_{CW1}	60		80		ns	
$\overline{CE}_2$ High to end of write	t_{CW2}	60		80		ns	
Address valid to end of write	t_{AW}	60		80		ns	
Address setup time	t_{AS}	0		0		ns	
Write pulse width	t_{WP}	55		75		ns	
Write recovery time	t_{WR}	0		0		ns	
Input data setup time	t_{DW}	30		40		ns	
Input data hold time	t_{DH}	0		0		ns	
$\overline{WE}$ High to output active	t_{WLZ}	5		5		ns	1
$\overline{WE}$ Low to output in High-Z	t_{HWZ}		30		35	ns	1
$\overline{OE}$ High to output in High-Z	t_{OHZ}		30		35	ns	1

NOTE:

- Active output to high-impedance and high-impedance to output active tests specified for a $\pm 200\text{ mV}$ transition from steady state levels into the test load.

TEST CONDITIONS

PARAMETER	MODE	NOTE
Input pulse levels	0.6 V to 2.4 V	
Input rise/fall times	5 ns	
Input/output timing levels	1.5 V	
Output load, timing test	1TTL + C_L (100 pF)	1

NOTE:

- Includes scope and jig capacitance.

PIN CAPACITANCE ($T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input capacitance	C_{IN}	$V_{IN} = 0\text{ V}$		10		pF	1
I/O capacitance	$C_{I/O}$	$V_{I/O} = 0\text{ V}$		10		pF	1

NOTE:

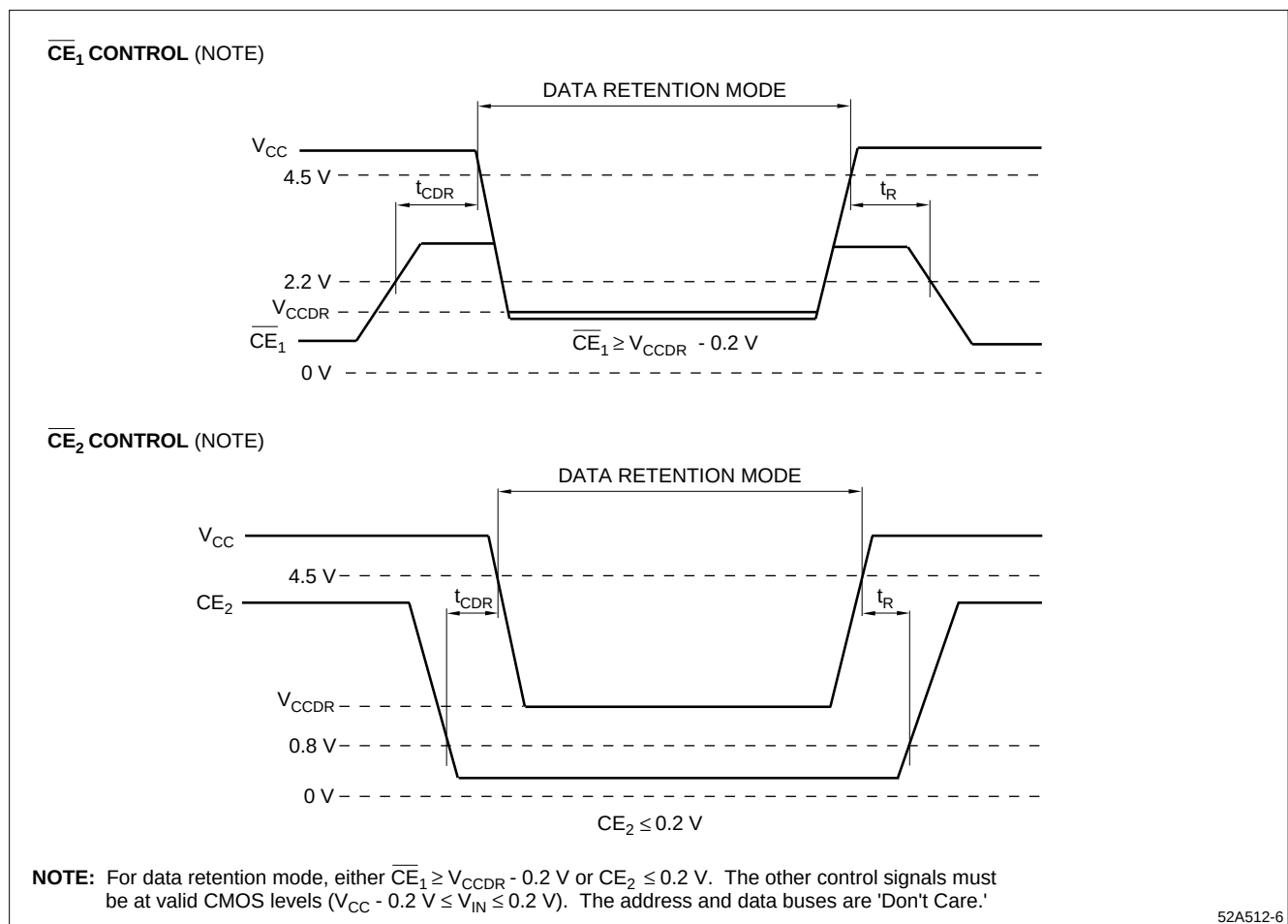
- This parameter is sampled and not production tested.

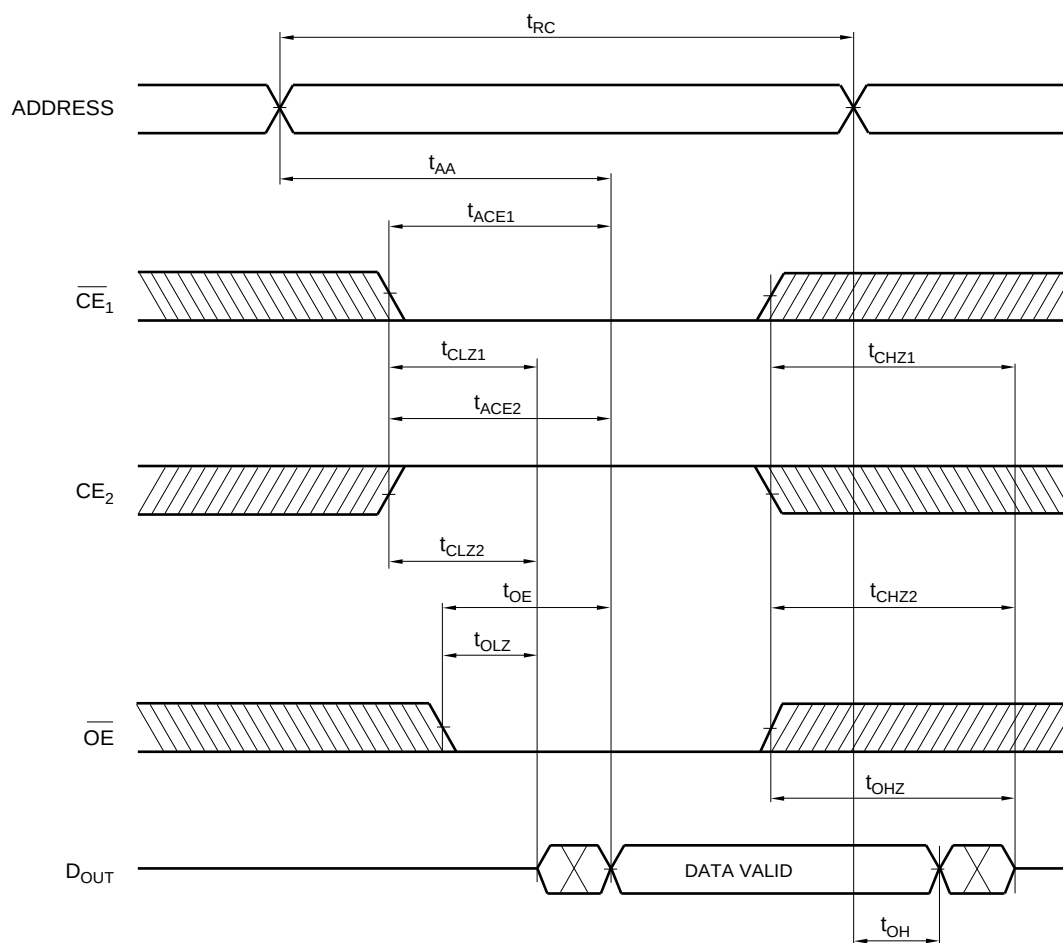
DATA RETENTION CHARACTERISTICS ($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Data retention supply voltage	V_{CCDR}	$\overline{CE}_2 \leq 0.2\text{ V}$ or $\overline{CE}_1 \geq V_{CCDR} - 0.2\text{ V}$	2.0	5.5	V	1
Data retention supply current	I_{CCDR}	$V_{CCDR} = 3.0\text{ V}$ $\overline{CE}_2 \leq 0.2\text{ V}$ or $\overline{CE}_1 \geq V_{CCDR} - 0.2\text{ V}$	$t_A = 25^\circ\text{C}$	1	μA	
			$t_A = 40^\circ\text{C}$	3		
				25		1
Chip enable setup time	t_{CDR}		0		ns	
Chip enable hold time	t_R		t_{RC}		ns	2

NOTES:

- $\overline{CE}_2 \geq V_{CCDR} - 0.2\text{ V}$ or $\overline{CE}_2 \leq 0.2\text{ V}$.
- t_{RC} = Read cycle time.

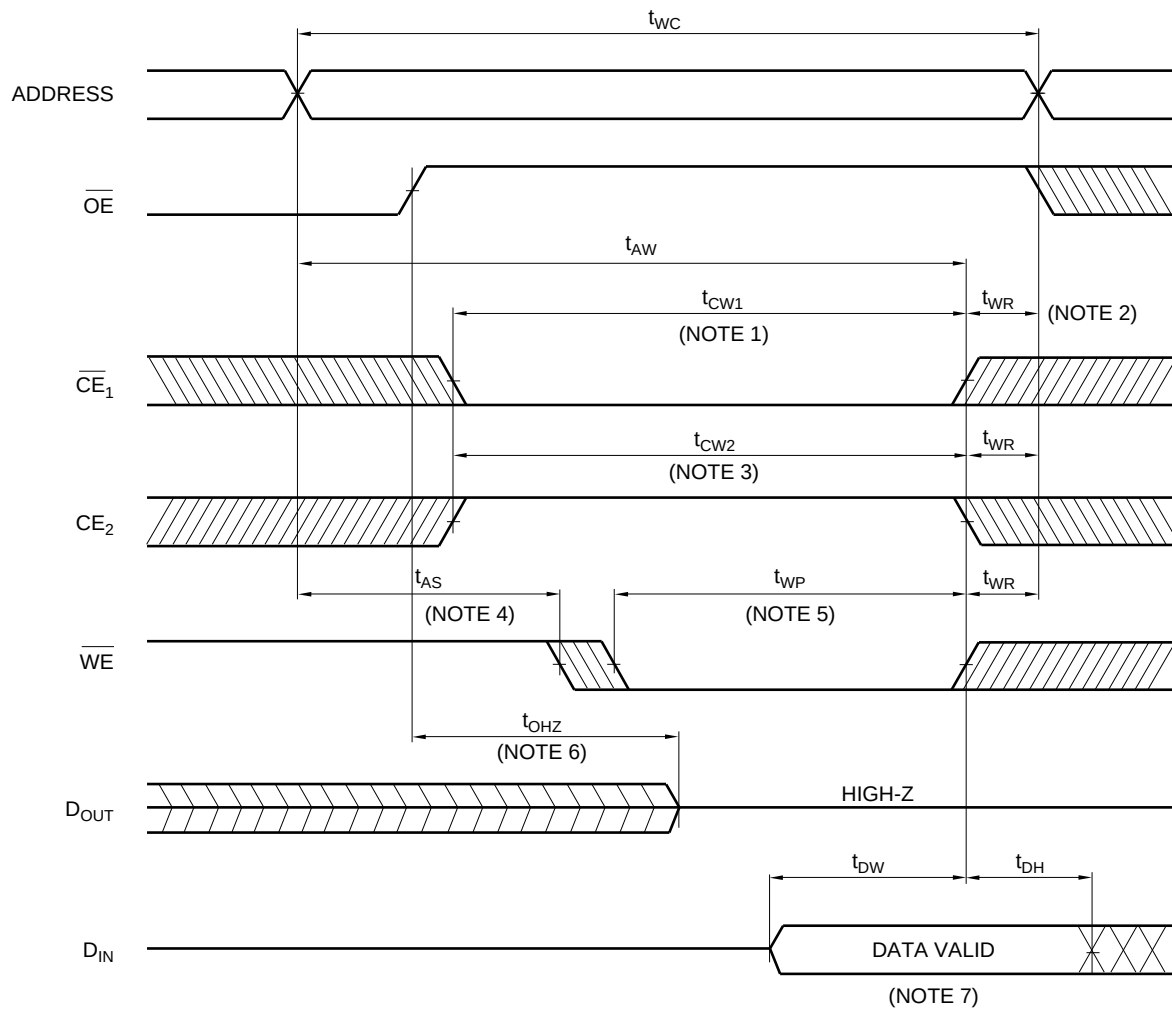
**Figure 4. Low Voltage Data Retention**



NOTE: $\overline{WE}$ is 'HIGH' level during the read cycle.

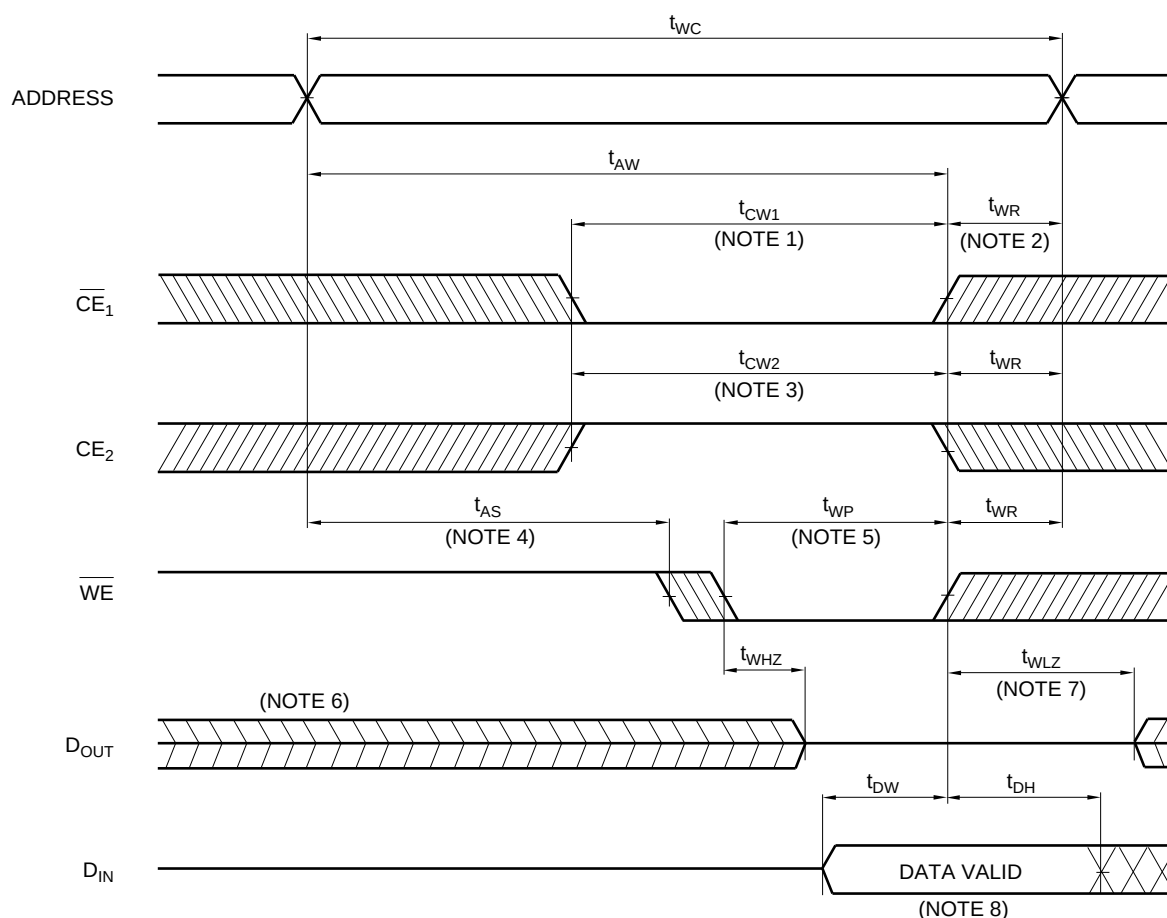
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Figure 5. Read Cycle



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Figure 6. Write Cycle – OE Controlled

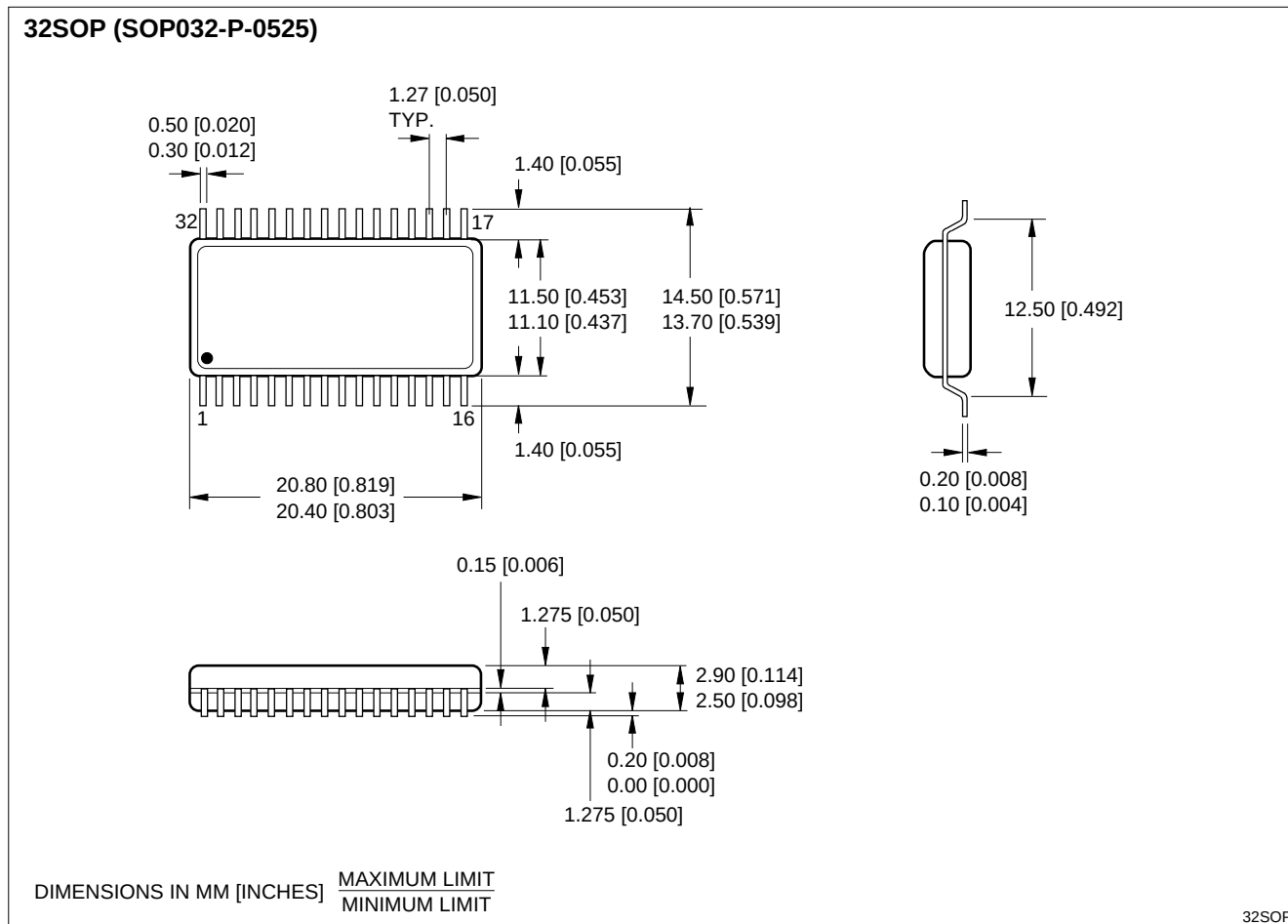
**NOTES:**

1. t_{CW1} is defined as the time from the last occurring transition, either $\overline{CE}_1$ LOW transition, to the time when the writing is finished.
2. t_{WR} is defined as the time from writing finish to address change.
3. t_{CW2} is defined as the time from the last occurring transition, either CE_2 HIGH transition, to the time when the writing is finished.
4. t_{AS} is defined as the time from address change to writing start.
5. The writing occurs during an overlapping period of $\overline{CE}_1 = \text{'LOW'}$, $CE_2 = \text{'HIGH'}$, and $\overline{WE} = \text{'LOW'}$ (t_{WP}).
6. If $\overline{CE}_1$ LOW transition, or CE_2 HIGH transition occurs at the same time or after $\overline{WE}$ LOW transition, the outputs will remain high-impedance.
7. If $\overline{CE}_1$ HIGH transition or CE_2 LOW transition occurs at the same time or before $\overline{WE}$ HIGH transition, the outputs will remain high-impedance.
8. When I/O pins are in the output state, input signals with the opposite logic level must not be applied.

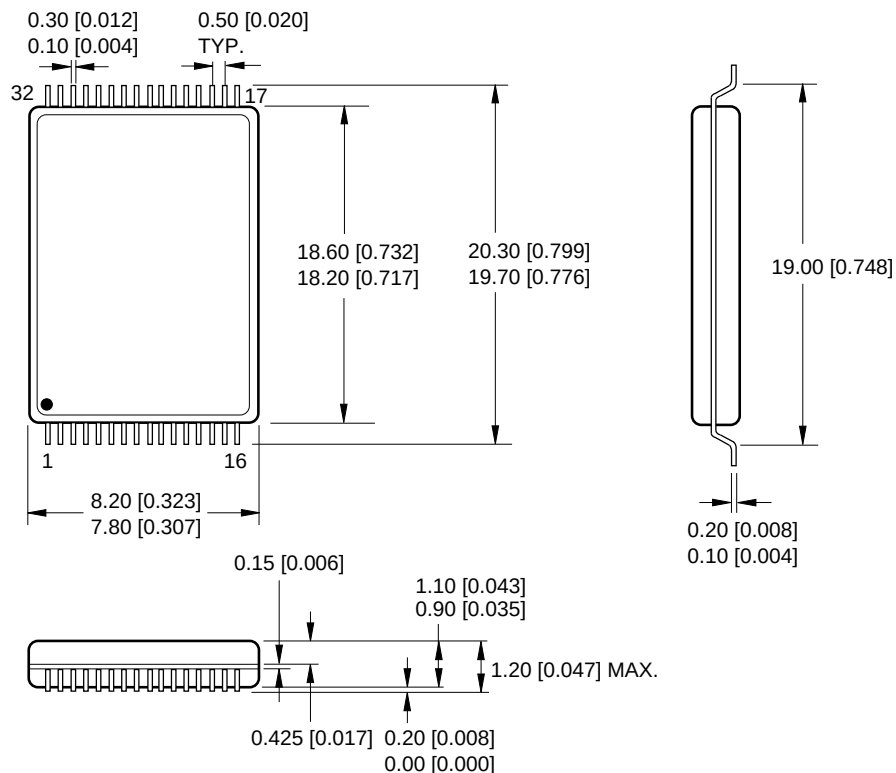
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Figure 7. Write Cycle – $\overline{OE}$ Low Fixed

PACKAGE DIAGRAMS



32-pin, 525-mil SOP

32TSOP (Type I) (TSOP032-P-0820)

DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT
MINIMUM LIMIT

32TSOP

32-pin, 8 × 20 mm² TSOP (Type I)**ORDERING INFORMATION**

LH52A512	X	- ##	LL
Device Type	Package	Speed	Power
			Low-Low-power standby
			{ 70 70 Access Time (ns) 10 100
			{ N 32-pin, 525-mil SOP (SOP032-P-0525) T 32-pin, 8 x 20 mm ² TSOP (Type I) (TSOP032-P-0820)
			CMOS 512K (64K x 8) Static RAM

Example: LH52A512N-70LL (CMOS 512K (64K x 8) Static RAM, 70 ns, Low-Low-power standby, 32-pin, 525-mil SOP)

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