

January 1999

**OBSOLETE PRODUCT
POSSIBLE SUBSTITUTE PRODUCT
HA-2525**

38MHz, Operational Amplifier

Features

- High Open Loop Gain at Video
Frequencies 42dB (Typ) at 1MHz
- Unity Gain
Crossover Frequency (f_T) 38MHz (Typ)
- Full Power Bandwidth
 $V_O = 18V_{P-P}$ 1.2MHz (Typ)
- Slew Rate
 - 20dB Amplifier 70V/ μ s (Typ)
 - Unity Gain Amplifier..... 25V/ μ s (Typ)
- Settling Time 0.6 μ s (Typ)
- Output Current..... $\pm 15mA$ (Min)
- Single Capacitor Compensation
- Offset Null Terminals

Applications

- Video Amplifiers
- Fast Peak Detectors
- Meter Driver Amplifiers
- High Frequency Feedback Amplifiers
- Video Pre-Drivers
- Oscillators
- Multivibrators
- Voltage Controlled Oscillator
- Fast Comparators

Description

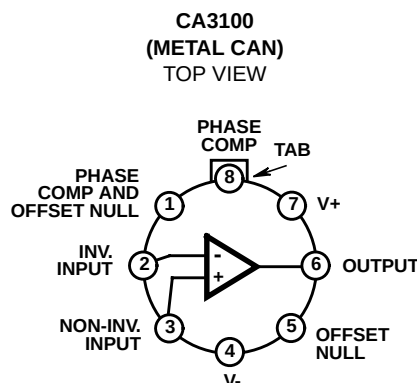
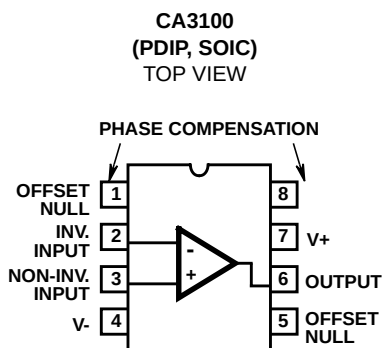
The CA3100 is a large signal wideband, high speed operational amplifier which has a unity gain cross over frequency (f_T) of approximately 38MHz and an open loop, 3dB corner frequency of approximately 110kHz. It can operate at a total supply voltage of from 14V to 36V ($\pm 7V$ to $\pm 18V$ when using split supplies) and can provide at least 18V_{P-P} and 30mA_{P-P} at the output when operating from $\pm 15V$ supplies. The CA3100 can be compensated with a single external capacitor and has DC offset adjust terminals for those applications requiring offset null. (See Figure 1).

The CA3100 circuit contains both bipolar and PMOS transistors on a single monolithic chip.

Part Number Information

PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA3100E	-40 to 85	8 Ld PDIP	E8.3
CA3100M (3100)	-40 to 85	8 Ld SOIC	M8.15
CA3100T	-55 to 125	8 Pin Metal Can	T8.C

Pinouts



CA3100

Absolute Maximum Ratings

Supply Voltage (Between V+ and V- Terminals) 36V
Differential Input Voltage 12V
Input Voltage to Ground V+ to V-
Offset Terminal to V- Terminal Voltage $\pm 0.5V$
Output Current (Note 2) 50mA

Operating Conditions

Temperature Range
CA3100E, CA3100M $-40^{\circ}C$ to $85^{\circ}C$
CA3100T $-55^{\circ}C$ to $125^{\circ}C$

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} ($^{\circ}C/W$) θ_{JC} ($^{\circ}C/W$)
PDIP Package 100 N/A
SOIC Package 165 N/A
Metal Can Package 170 85
Maximum Junction Temperature (Metal Can) $175^{\circ}C$
Maximum Junction Temperature (Plastic Package) $150^{\circ}C$
Maximum Storage Temperature Range $-65^{\circ}C$ to $150^{\circ}C$
Maximum Lead Temperature (Soldering 10s) $300^{\circ}C$
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
2. CA3100 does not contain circuitry to protect against short circuits in the output.

Electrical Specifications $T_A = 25^{\circ}C$, $V_{SUPPLY} = \pm 15V$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DC						
Input Offset Voltage	V_{IO}	$V_O = 0 \pm 0.1V$	-	± 1	± 5	mV
Input Bias Current	I_{IB}	$V_O = 0 \pm 1V$	-	0.7	2	μA
Input Offset Current	I_{IO}	$V_O = 0 \pm 1V$	-	± 0.05	± 0.4	μA
Common Mode Input Voltage Range	V_{ICR}	$CMRR \geq 76dB$	± 12	+14 -13	-	V
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm 12V$	76	90	-	dB
Maximum Output Voltage	V_{OM}^{+}	Differential Input Voltage = $0 \pm 0.1V$, $R_L = 2k\Omega$	+9	+11	-	V
	V_{OM}^{-}		-9	-11	-	V
Maximum Output Current	I_{OM}^{+}	Differential Input Voltage = $0 \pm 0.1V$, $R_L = 250\Omega$	+15	+30	-	mA
	I_{OM}^{-}		-15	-30	-	mA
Supply Current	I^{+}	$V_O = 0 \pm 0.1V$, $R_L \geq 10k\Omega$	-	8.5	10.5	mA
Power Supply Rejection Ratio	PSRR	$\Delta V^{+} = \pm 1V$, $\Delta V^{-} = \pm 1V$	60	70	-	dB
DYNAMIC						
Unity-Gain Crossover Frequency	f_T	$C_C = 0$, $V_O = 0.3V_{P-P}$	-	38	-	MHz
Open Loop Voltage Gain	A_{OL}	$f = 1kHz$, $V_O = \pm 1V$, (Note 3)	56	61	-	dB
		$f = 1MHz$, $C_C = 0$, $V_O = 10V_{P-P}$	36	42	-	dB
Slew Rate	SR	$A_V = 10$, $C_C = 0$, $V_I = 1V$ (Pulse)	50	70	-	V/ μs
		$A_V = 1$, $C_C = 10pF$, $V_I = 10V$ (Pulse)	-	25	-	V/ μs
Full Power Bandwidth (Note 4)	FPBW	$A_V = 10$, $C_C = 0$, $V_O = 18V_{P-P}$	0.8	1.2	-	MHz
		$A_V = 1$, $C_C = 10pF$, $V_O = 18V_{P-P}$	-	0.4	-	MHz
Open Loop Differential Input Impedance	Z_I	$f = 1MHz$	-	30	-	$k\Omega$
Open Loop Output Impedance	Z_O	$f = 1MHz$	-	110	-	Ω

CA3100

Electrical Specifications $T_A = 25^\circ\text{C}$, $V_{\text{SUPPLY}} = \pm 15\text{V}$, Unless Otherwise Specified (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Wideband Noise Voltage (RTI)	e_N (Total)	$\text{BW} = 1\text{MHz}$, $R_S = 1\text{k}\Omega$	-	8	-	μVRMS
Settling Time (To Within $\pm 50\text{mV}$ of 9V Output Swing)	t_S	$R_L = 2\text{k}\Omega$, $C_L = 20\text{pF}$	-	0.6	-	μs

NOTES:

3. Low frequency dynamic characteristic.

4. Full Power Bandwidth = $\frac{\text{Slew Rate}}{\pi V_{\text{OP-P}}}$.

Test Circuits

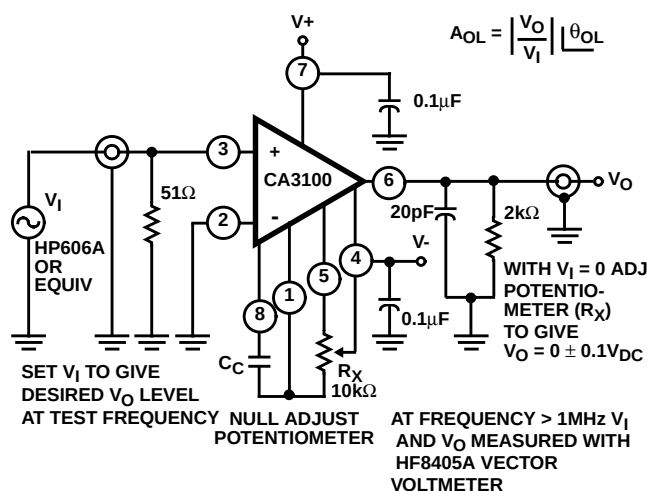


FIGURE 1. OPEN-LOOP VOLTAGE GAIN TEST CIRCUIT AND OFFSET ADJUST CIRCUIT

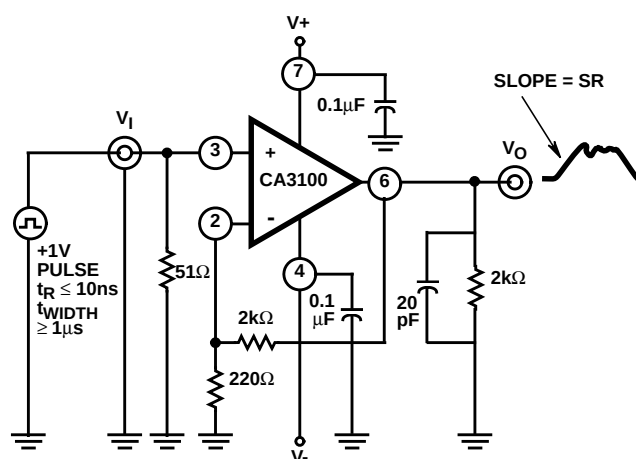


FIGURE 2. SLEW RATE IN 10X AMPLIFIER TEST CIRCUIT

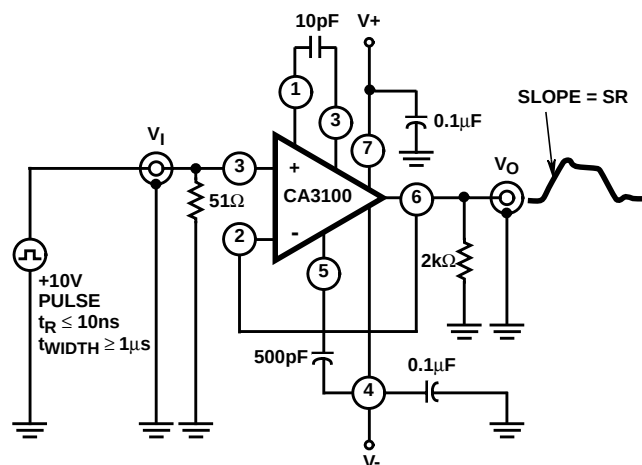


FIGURE 3. FOLLOWER SLEW RATE TEST CIRCUIT

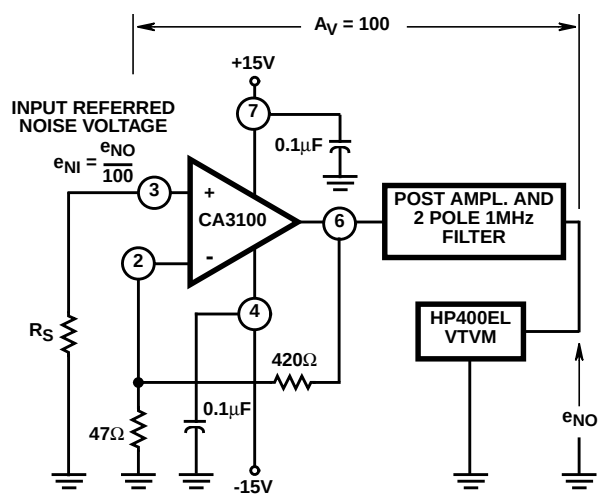


FIGURE 4. WIDEBAND INPUT NOISE VOLTAGE TEST CIRCUIT

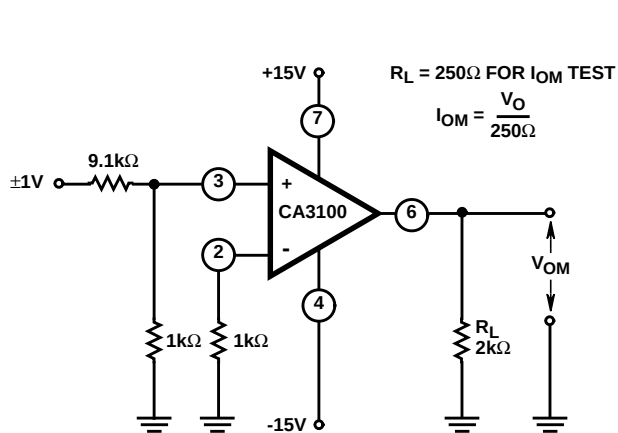
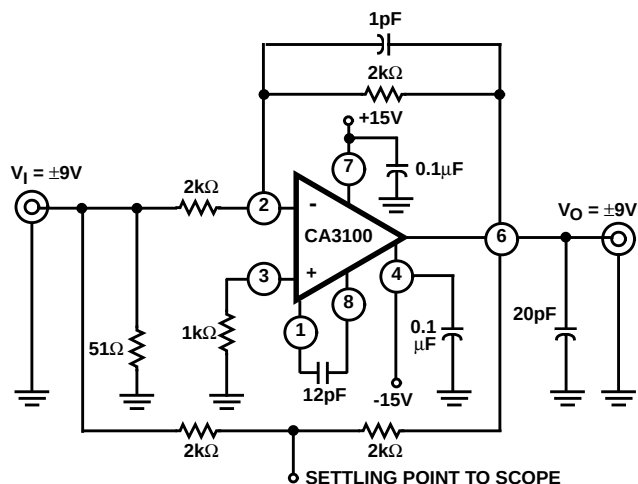
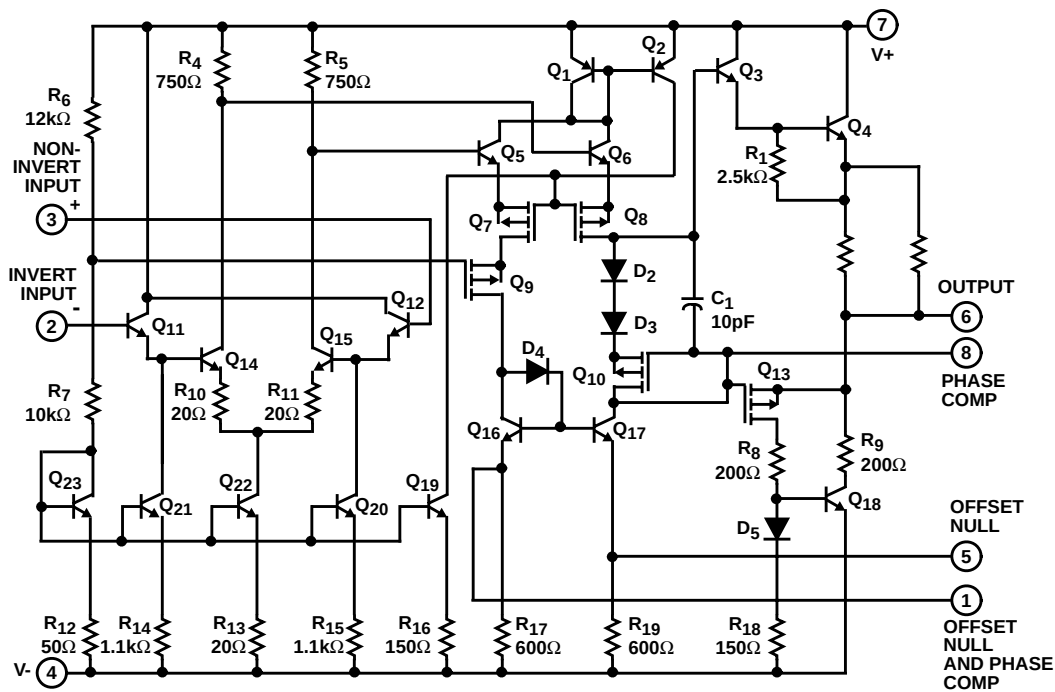
Test Circuits (Continued)FIGURE 5. OUTPUT VOLTAGE SWING (V_{OM}), OUTPUT CURRENT SWING (I_{OM}) TEST CIRCUIT

FIGURE 6. SETTLING TIME TEST CIRCUIT

Schematic Diagram

Typical Applications

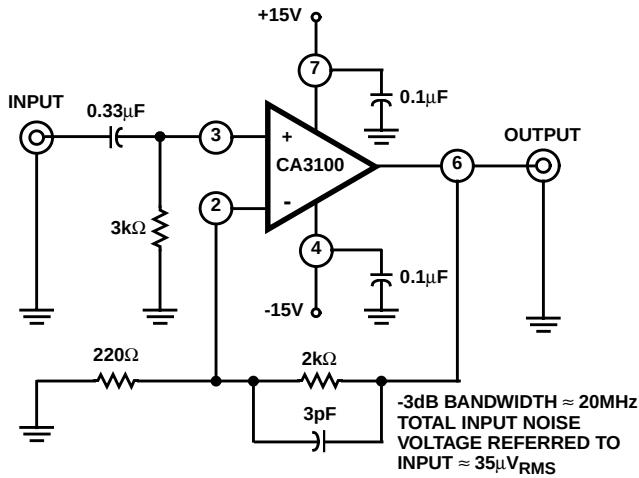


FIGURE 7. 20dB VIDEO AMPLIFIER

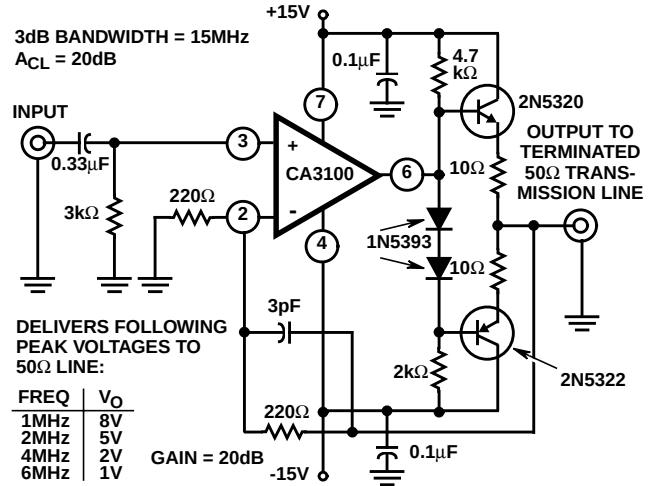


FIGURE 8. 20dB VIDEO LINE DRIVER

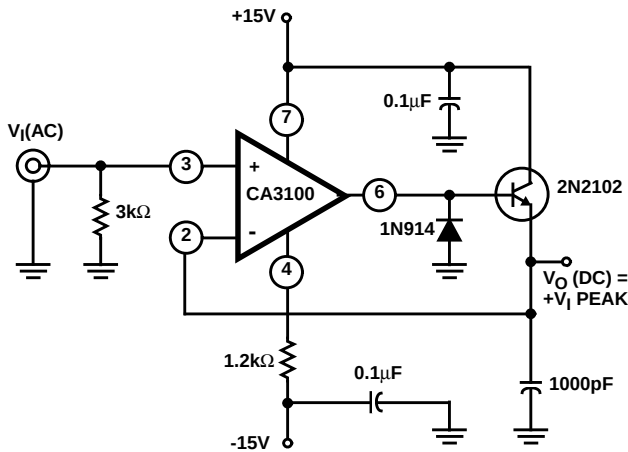


FIGURE 9. FAST POSITIVE PEAK DETECTOR

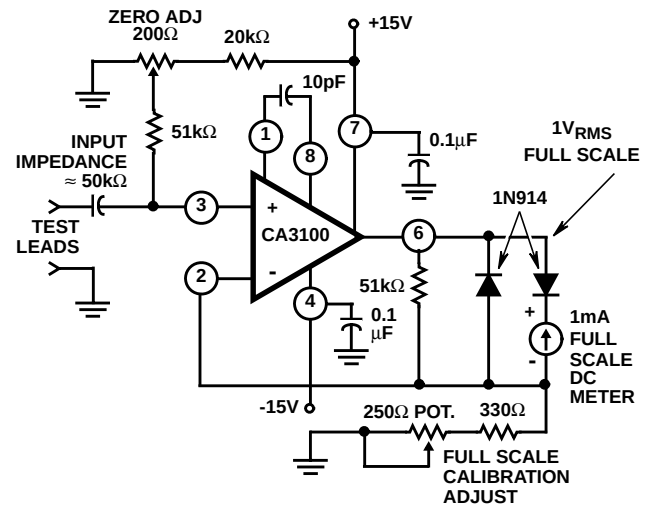


FIGURE 10. 1MHz METER-DRIVER AMPLIFIER

Typical Performance Curves

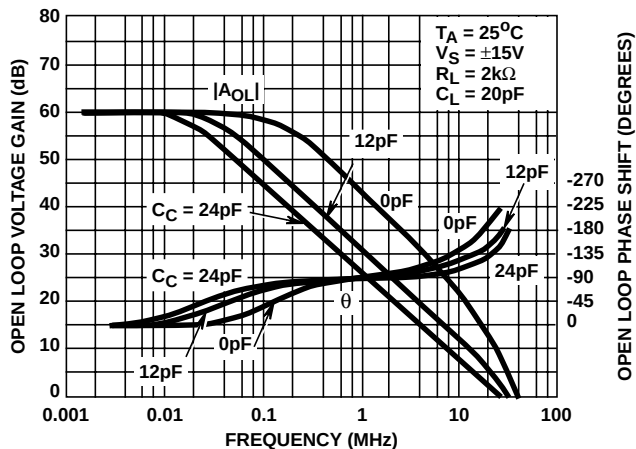


FIGURE 11. OPEN LOOP GAIN, OPEN LOOP PHASE SHIFT vs FREQUENCY

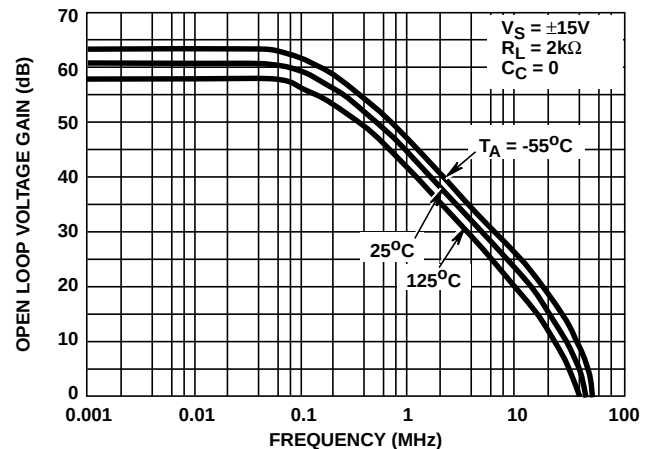


FIGURE 12. OPEN LOOP GAIN vs FREQUENCY

Typical Performance Curves (Continued)

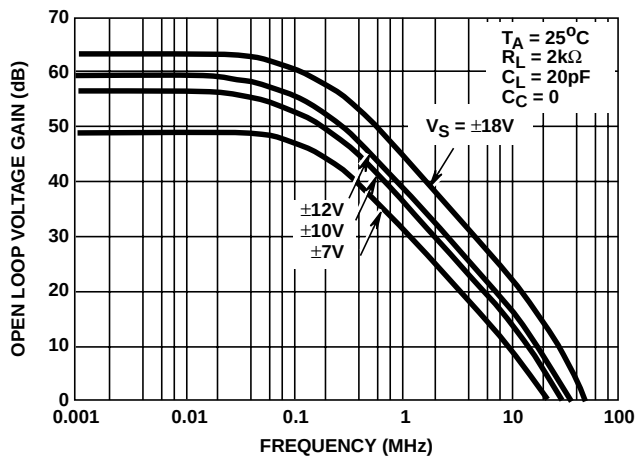


FIGURE 13. OPEN LOOP GAIN vs FREQUENCY

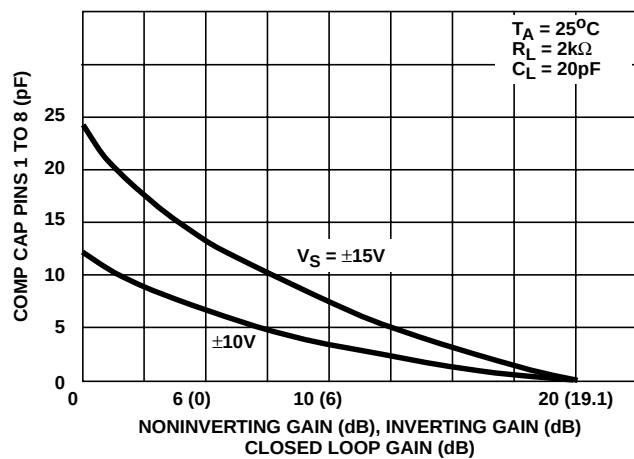


FIGURE 14. REQUIRED COMPENSATION CAPACITANCE vs CLOSED LOOP GAIN

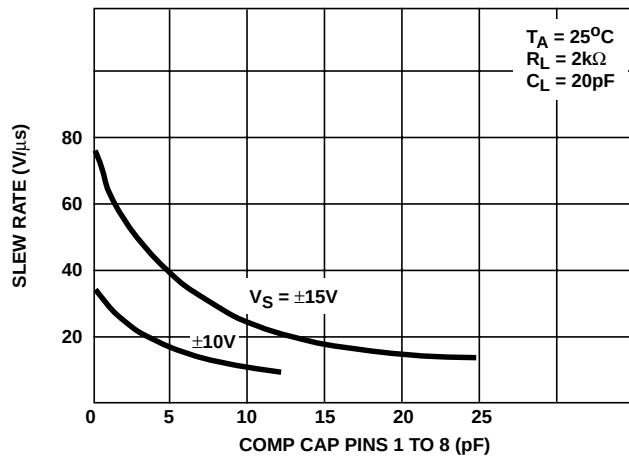


FIGURE 15. SLEW RATE vs COMPENSATION CAPACITANCE

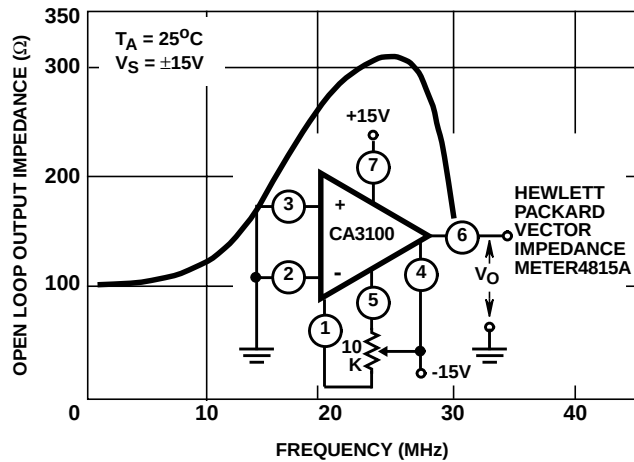


FIGURE 16. TYPICAL OPEN LOOP OUTPUT IMPEDANCE vs FREQUENCY

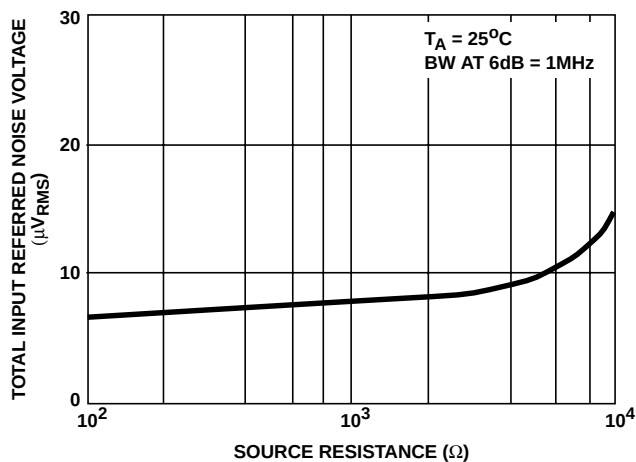


FIGURE 17. WIDEBAND INPUT NOISE VOLTAGE vs SOURCE RESISTANCE

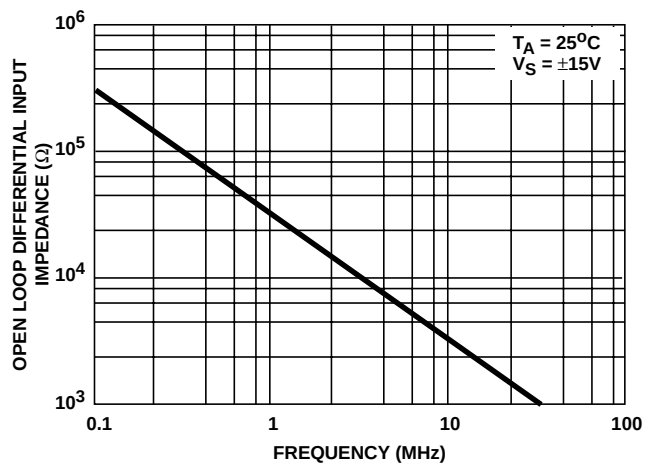


FIGURE 18. TYPICAL OPEN LOOP DIFFERENTIAL INPUT IMPEDANCE vs FREQUENCY

Typical Performance Curves (Continued)

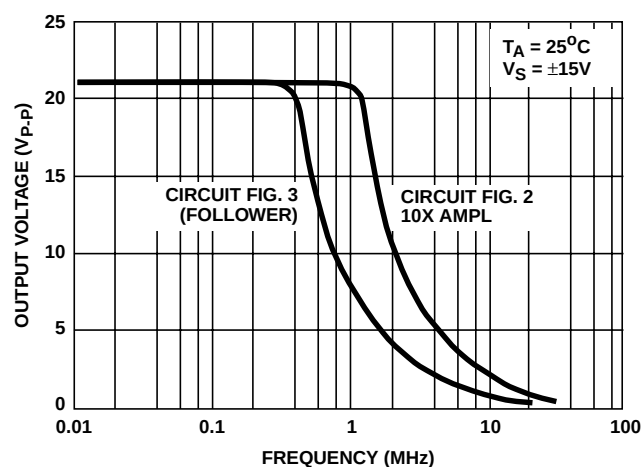


FIGURE 19. MAXIMUM OUTPUT VOLTAGE SWING vs FREQUENCY

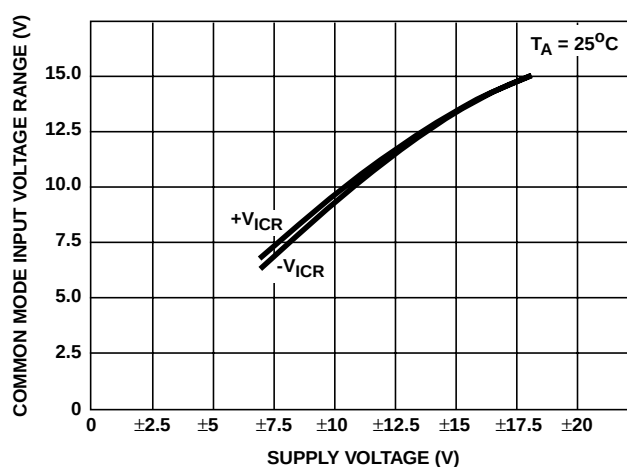


FIGURE 20. COMMON MODE INPUT VOLTAGE RANGE vs SUPPLY VOLTAGE

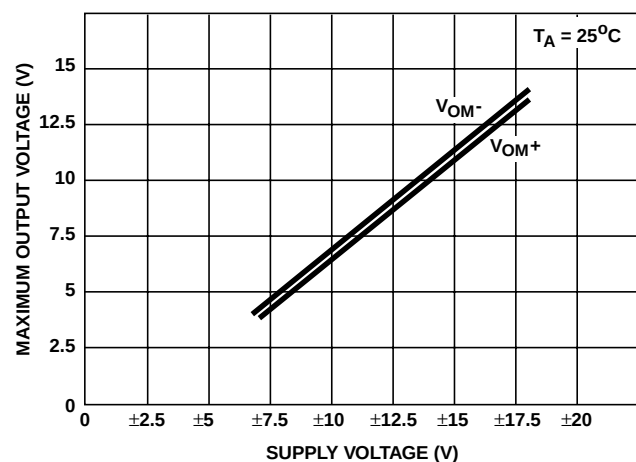


FIGURE 21. MAXIMUM OUTPUT VOLTAGE vs SUPPLY VOLTAGE

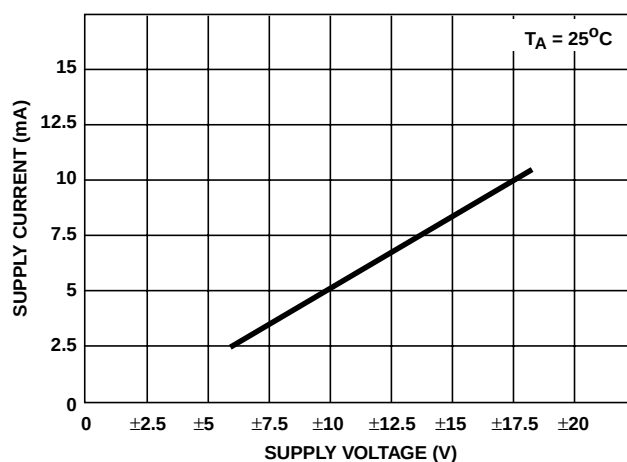


FIGURE 22. SUPPLY CURRENT vs SUPPLY VOLTAGE

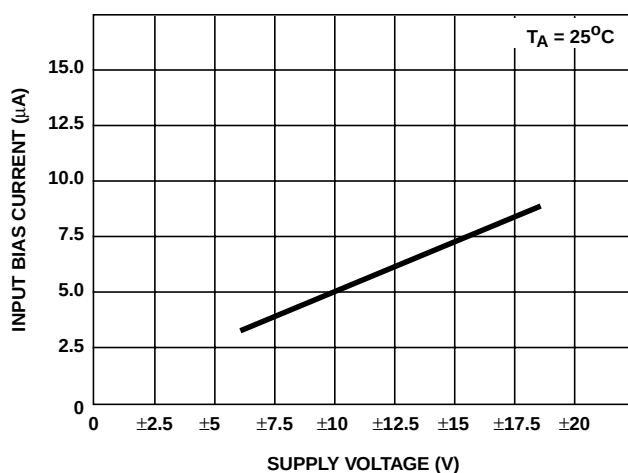


FIGURE 23. INPUT BIAS CURRENT vs SUPPLY VOLTAGE