

LH5118

CMOS 16K (2K × 8) Static RAM

FEATURES

- 2,048 × 8 bit organization
- Access time: 100 ns (MAX.)
- Power consumption:
 - Operating: 220 mW (MAX.)
 - Standby: 5.5 μ W (MAX.)
- Single +5 V power supply
- Fully-static operation
- TTL compatible I/O
- Three-state outputs
- Wide temperature range available
LH5118H: -40 to +85°C
- Packages:
 - 24-pin, 600-mil DIP
 - 24-pin, 300-mil SK-DIP
 - 24-pin, 450-mil SOP

DESCRIPTION

The LH5118 is a static RAM organized as 2,048 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

The LH5118 accepts two chip-enables. These allow data to be held with battery back-up for memory expansion (used in systems with multiple memory devices).

Low power mode (I_{SB}) is available with $\overline{CE}_1$ and $\overline{CE}_2$ deactivated.

PIN CONNECTIONS

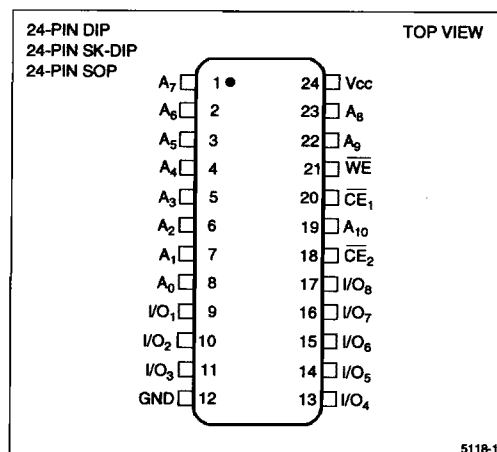


Figure 1. Pin Connections for DIP, SK-DIP, and SOP Packages

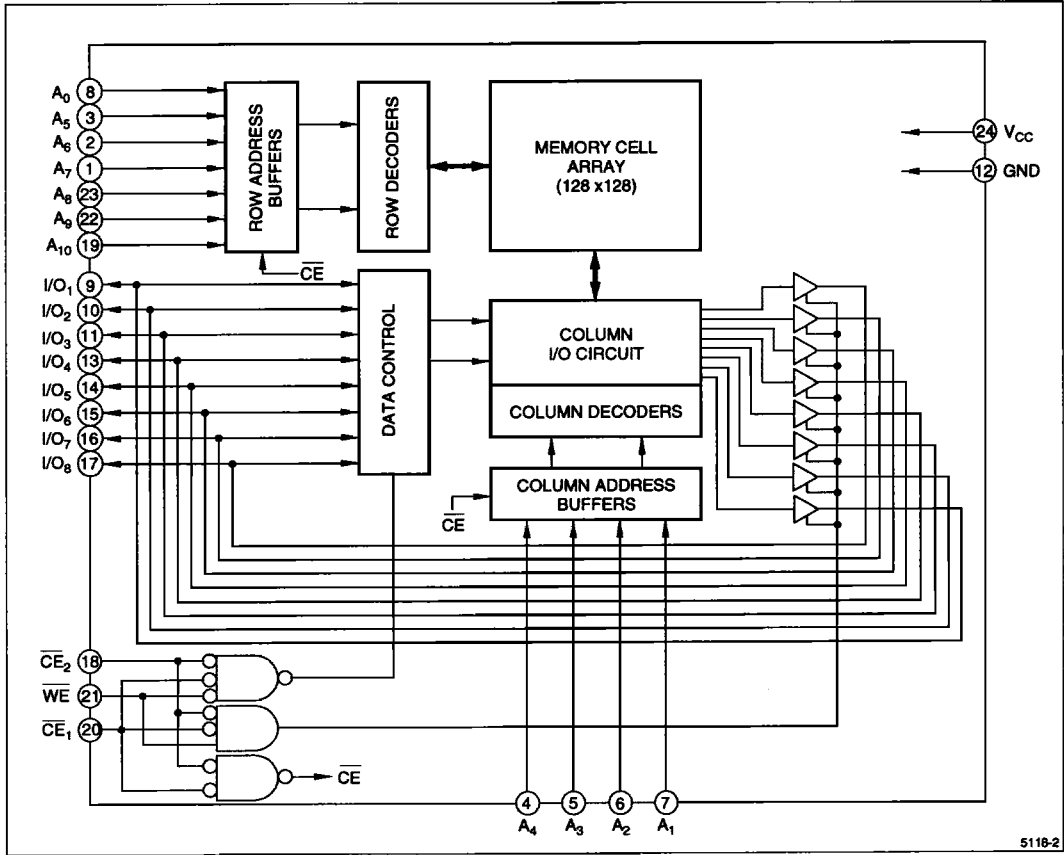


Figure 2. LH5118 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A ₀ - A ₁₀	Address input
$\overline{CE}_2$	Chip Enable input no. 2
$\overline{CE}_1$	Chip Enable input no. 1
$\overline{WE}$	Write Enable input

SIGNAL	PIN NAME
I/O ₁ - I/O ₈	Data Input/Output
V _{CC}	Power supply
GND	Ground

TRUTH TABLE

$\overline{CE}_1$	$\overline{CE}_2$	$\overline{WE}$	MODE	I/O ₁ - I/O ₈	SUPPLY CURRENT	NOTE
X	H	X	Deselect	High-Z	Standby (I _{SB})	1
H	X	X	Deselect	High-Z	Standby (I _{SB})	1
L	L	L	Write	D _{IN}	Operating (I _{CC})	
L	L	H	Read	D _{OUT}	Operating (I _{CC})	

NOTE:

1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to $V_{CC} + 0.3$	V	1
Operating temperature	T_{opr}	0 to +70	°C	2
		-40 to +85		3
Storage temperature	T_{stg}	-55 to +150	°C	

NOTES:

1. The maximum applicable voltage on any pin with respect to GND.
2. Applied to the LH5118/D/N
3. Applied to the LH5118H/HD/HN

RECOMMENDED OPERATING CONDITIONS ¹

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.2		$V_{CC} + 0.3$	V
	V_{IL}	-0.3		0.8	V

NOTE:

1. $T_A = 0$ to +70°C (LH5118/D/N), $T_A = -40$ to +85°C (LH5118H/HD/HN)

DC CHARACTERISTICS ¹ ($V_{CC} = 5\text{ V} \pm 10\%$)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Output 'LOW' voltage	V_{OL}	$I_{OL} = 2.1\text{ mA}$			0.4	V	
Output 'HIGH' voltage	V_{OH}	$I_{OH} = -1.0\text{ mA}$	2.4			V	
Input leakage current	$ I_{II} $	$V_{IN} = 0\text{ V to } V_{CC}$			1.0	μA	
Output leakage current	$ I_{ILO} $	$\overline{CE}_2 = V_{IH}$ or $\overline{CE}_1 = V_{IH}$, $V_{IO} = 0\text{ V to } V_{CC}$			1.0	μA	
Operating current	I_{CC1}	Outputs open ($\overline{WE} = V_{CC}$)		25	30	mA	2
	I_{CC2}	Outputs open ($\overline{WE} = V_{IH}$)		30	40	mA	3
Standby current	I_{SB}	(1) $\overline{CE}_2 \geq V_{CC} - 0.2\text{ V}$, and ($\overline{CE}_1 \geq V_{CC} - 0.2\text{ V}$ or $\overline{CE}_1 \leq 0.2\text{ V}$) or			1.0	μA	
		(2) $\overline{CE}_1 \geq V_{CC} - 0.2\text{ V}$, and ($\overline{CE}_2 \geq V_{CC} - 0.2\text{ V}$ or $\overline{CE}_2 \leq 0.2\text{ V}$) All other inputs = 0 V to V_{CC}			0.2	μA	4

NOTES:

1. $T_A = 0$ to +70°C (LH5118/D/N), $T_A = -40$ to +85°C (LH5118H/HD/HN)
2. $\overline{CE}_2 = \overline{CE}_1 = 0\text{ V}$; all other input pins = 0 V to V_{CC}
3. $\overline{CE}_2 = \overline{CE}_1 = V_{IL}$; all other input pins = V_{IL} to V_{IH}
4. $T_A = 25^\circ\text{C}$

AC CHARACTERISTICS¹**(1) READ CYCLE ($V_{CC} = 5\text{ V} \pm 10\%$)**

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	100			ns	
Address access time	t_{AA}			100	ns	
$\overline{CE}_1$ access time	t_{ACE1}			100	ns	
$\overline{CE}_2$ access time	t_{ACE2}			100	ns	
$\overline{CE}_1$ Low to output in Low-Z	t_{CLZ1}	10			ns	2
$\overline{CE}_2$ Low to output in Low-Z	t_{CLZ2}	10			ns	2
$\overline{CE}_1$ to output in High-Z	t_{CHZ1}	0		40	ns	2
$\overline{CE}_2$ to output in High-Z	t_{CHZ2}	0		40	ns	2
Data hold time	t_{OH}	10			ns	

(2) WRITE CYCLE ($V_{CC} = 5\text{ V} \pm 10\%$)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Write cycle time	t_{WC}	100			ns	
Chip enable to end of write	t_{CW}	80			ns	
Address valid time	t_{AW}	80			ns	
Address setup time	t_{AS}	0			ns	
Write pulse width	t_{WP}	60			ns	
Write recovery time	t_{WR}	10			ns	
$\overline{WE}$ Low to output in High-Z	t_{WHZ}			30	ns	2
Data valid to end of write	t_{DW}	30			ns	
Data hold time	t_{DH}	10			ns	
Output active from end of write	t_{OW}	10			ns	2

NOTES:

- $T_A = 0$ to $+70^\circ\text{C}$ (LH5118/D/N), $T_A = -40$ to $+85^\circ\text{C}$ (LH5118H/HD/HN)
- Active output to high-impedance and high-impedance to output active tests specified for a $\pm 500\text{ mV}$ transition from steady state levels into the test load. $C_{LOAD} = 5\text{ pF}$.

AC TEST CONDITIONS

PARAMETER	MODE
Input voltage amplitude	0.8 V to 2.2 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output load condition	1TTL + 100 pF

DATA RETENTION CHARACTERISTICS ¹

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Data retention voltage	V _{CCDR}	$\overline{CE}_1 \geq V_{CCDR} - 0.2 \text{ V}$ or $\overline{CE}_2 \geq V_{CCDR} - 0.2 \text{ V}$	2.0			V	
Data retention current	I _{CCDR}	$\overline{CE}_1 \geq V_{CCDR} - 0.2 \text{ V}$, and ($\overline{CE}_2 \geq V_{CCDR} - 0.2 \text{ V}$ or $\overline{CE}_2 \leq 0.2 \text{ V}$) or $\overline{CE}_2 \geq V_{CCDR} - 0.2 \text{ V}$, and ($\overline{CE}_1 \geq V_{CCDR} - 0.2 \text{ V}$ or $\overline{CE}_1 \leq 0.2 \text{ V}$) V _{CCDR} = 3.0 V			1.0	μA	
					0.2		2
Chip disable to data retention	t _{CDR}		0			ns	
Recovery time	t _R		t _{RC}			ns	3

NOTES:

1. T_A = 0 to +70°C (LH5118/D/N), T_A = -40 to +85°C (LH5118H/HD/HN)
2. T_A = 25°C
3. t_{RC} = Read cycle time

CAPACITANCE ¹ (f = 1MHz, T_A = 25°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C _{IN}	V _{IN} = 0 V			7	pF
Input/output capacitance	C _{I/O}	V _{I/O} = 0 V			10	pF

NOTE:

1. This parameter is sampled and not production tested.

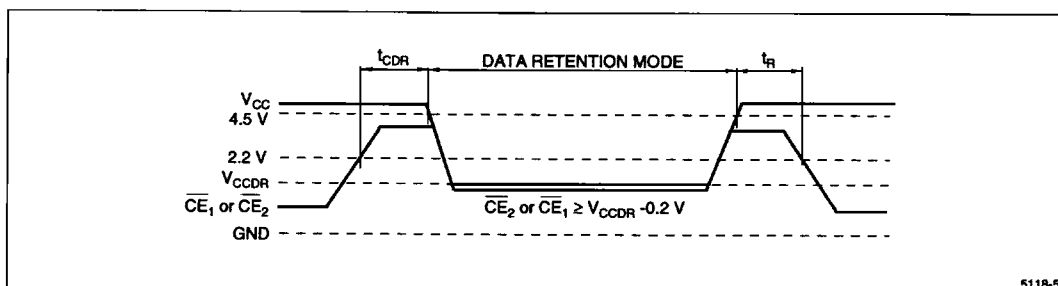


Figure 3. Low Voltage Data Retention

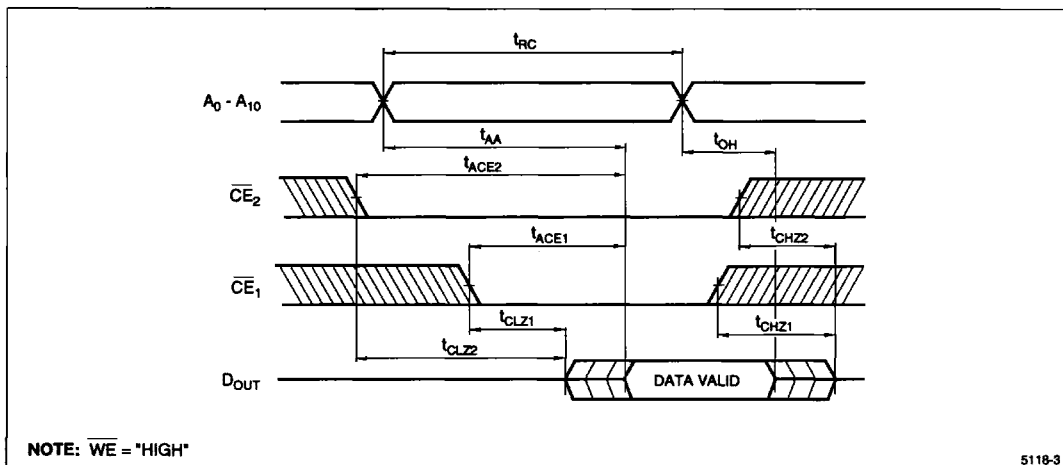


Figure 4. Read Cycle

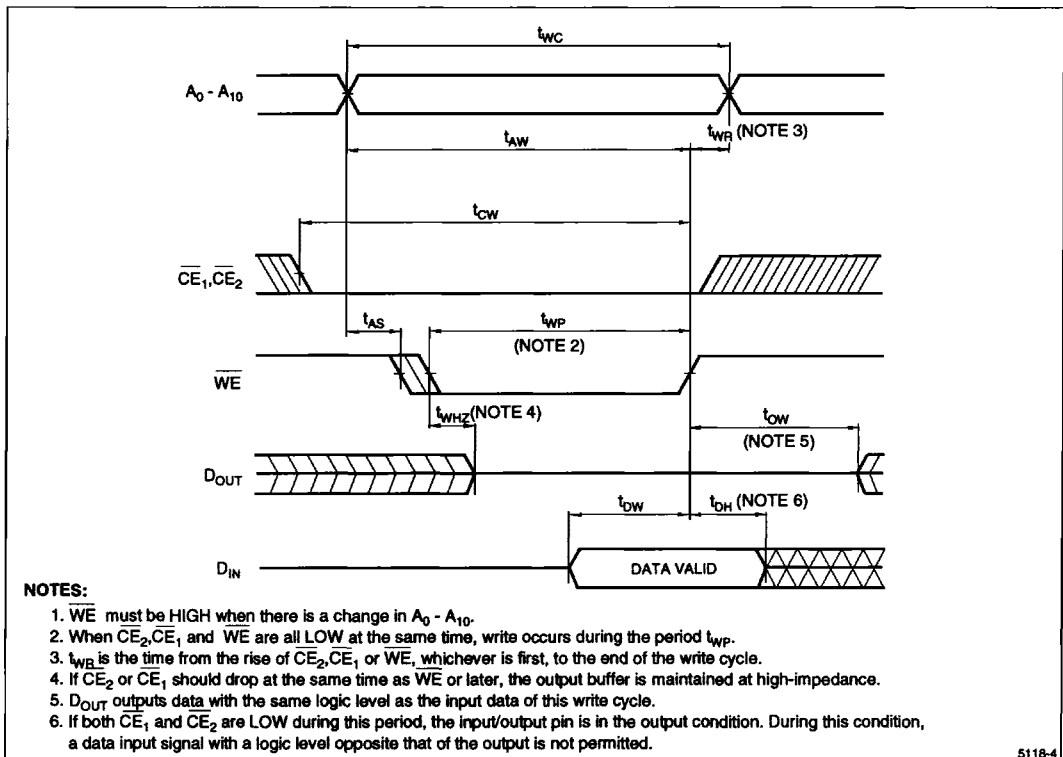
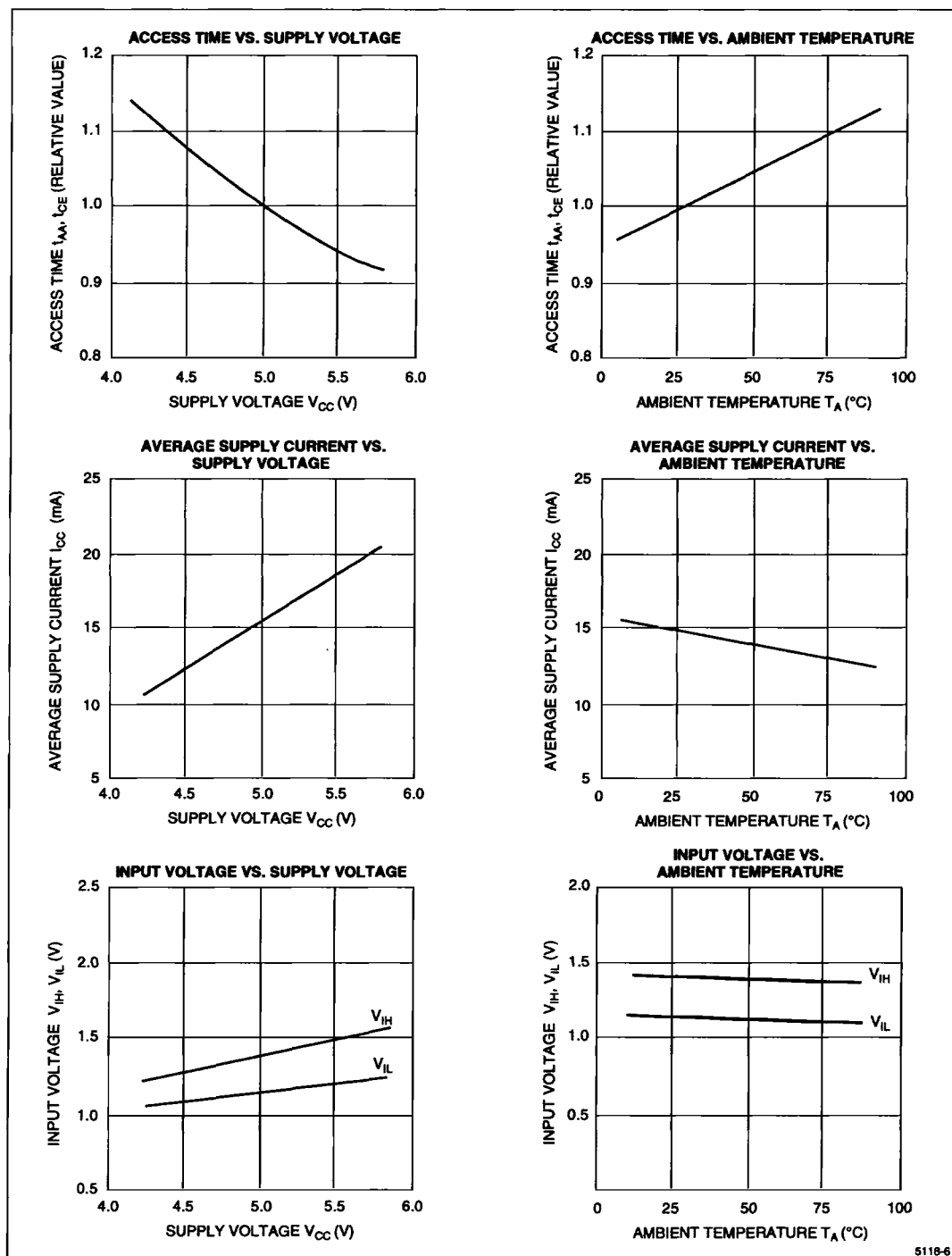
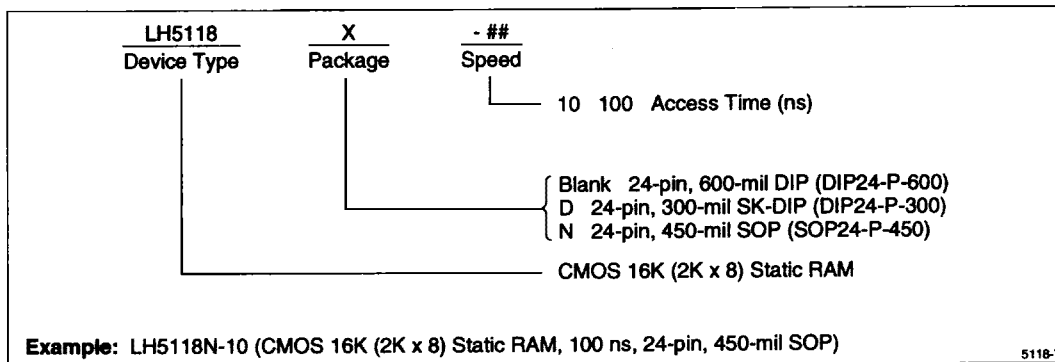


Figure 5. Write Cycle (Note 1)



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Figure 6. Electrical Characteristic Curves
($V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ Unless Otherwise Specified)

ORDERING INFORMATION ($T_A = 0$ to $+70^\circ\text{C}$)**ORDERING INFORMATION ($T_A = -40$ to $+85^\circ\text{C}$)**